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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,747	04/23/2001	Howard Sachs	021111000100	4810

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EXAMINER	
BOWERS, BRANDON	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,747	SACHS, HOWARD	
	Examiner	Art Unit	
	Brandon W Bowers	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-64* is/are pending in the application.

4a) Of the above claim(s) *1-32 and 44-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 33-43 in the reply filed on 2 July
VS 2004 is acknowledged. Applicant is requested to cancel all non-elected claims.

Claim Objections

Claims 40, 42 is objected to because of the following informalities: In claim 42, the limitation "on the order of 1000 gates" is indefinite. Are 500 gates "on the order of 1000 gates"? Is 100? Is 5000? Maybe, maybe not. In claim 40, GDSIII should be GDSII. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 33-37, 40, and 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guruswamy et al., US Patent No. 5,984,510 in view of Crafts, US Patent No. 5,671,397 and Dangelo et al, US Patent No 5,880,971.

In reference to claim 33, Guruswamy teaches a method of designing an integrated circuit comprising creating a netlist design for each of a set of sub-circuits (Figure 4, 136), creating a physical layout for each such sub-circuit which layout

includes information defining the physical position of all components of the sub-circuit (Figure 4, 144), and locations on each such sub-circuit for interconnecting such sub-circuit to at least one other circuit (Figure 7, 174/173), defining desired electrical interconnections among all of the components of the sub-circuit (Figure 4, 154, defining interconnection information for providing electrical connections as needed among such components (Figure 2, 102), optimizing the design and layout for each such sub-circuit to obtain a desired level of operating speed for such sub-circuit independently of any use of such sub-circuit with any other sub-circuit(column 8, line 57 – column 9, line 4) storing such optimized design for later use in conjunction with other sub-circuits and other circuits (Figure 5, 92), creating a netlist design for the integrated circuit which includes at least two sub-circuits previously optimized and stored (Figure 5, 114), creating a physical layout for the integrated circuit by placing the at least two sub-circuits on a design in proximity to each other wherein the layout includes information defining the physical position of the at least two sub-circuits and the locations on each such sub-circuit for interconnecting such sub-circuit to at least one other circuit (Figure 5, 130); and defining desired electrical interconnections among the sub-circuits (Figure 5, 130). Guruswamy does not teach wherein in creating a netlist design for each of a set of sub-circuits, each sub-circuit has at least 300 gates. Guruswamy does not teach wherein in defining desired electrical interconnections among all of the components of the sub-circuit, the electrical connections are defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be designed later. Guruswamy does not teach wherein in defining desired electrical interconnections

among the sub-circuits, the electrical connections are defined entirely on layers other than the layers used for the desired electrical interconnections among the components of the sub-circuits. Crafts teaches teach wherein in defining desired electrical interconnections among all of the components of a sub-circuit, the electrical connections are defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be designed later and wherein in defining desired electrical interconnections among sub-circuits, the electrical connections are defined entirely on layers other than the layers used for the desired electrical interconnections among the components of the sub-circuits (column 1, lines 8-14). Dangelo teaches wherein circuit groups are less than a few thousand gates (column 13, line 42). Accordingly, it would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Dangelo and Craft into the method of Guruswamy to make a method for designing an integrated circuit comprising all the steps claimed in claim 33 because it removes obstacles to the free routing of global interconnects over a cell and because the seemingly insurmountable job of designing a highly complex circuit is broken into small, workable design projects of a few thousand gates.

In reference to claim 34, Craft teaches wherein in defining desired electrical interconnections among ~~all~~ all of the components of the sub-circuit, the electrical connections being defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be desired later, at least one layer of the electrical interconnections does not include both power and clock signals (column 1, lines 8-14).

In reference to claim 35, Guruswamy teaches wherein the plurality of layers are each layers having electrically conductive material thereon with vias between at least two adjoining layers (column 14, lines 40-49).

In reference to claim 36, Guruswamy teaches wherein each sub-circuit has a predefined size and shape (Figure 9).

In reference to claim 37, Guruswamy teaches wherein each sub-circuits has predefined interconnection locations for connecting that sub-circuit to at least one other sub-circuit (column 12, lines 1-9).

In reference to claim 40, Guruswamy teaches wherein each sub-circuit comprises a physical representation of a logic circuit (Figure 4, 170).

In reference to claim 42, Dangelo teaches wherein each sub-circuit comprises a few thousand gates.

In reference to claim 43, Craft teaches wherein no layer in the layers available for the provision of interconnections in an integrated circuit to be designed later includes both electrical connections for interconnecting components of the sub-circuit and electrical connections for connecting one sub-circuit to another (column 1, lines 8-14).

Claims 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guruswamy et al., US Patent No. 5,984,510 in view of Crafts, US Patent No. 5,671,397, and Dangelo et al, US Patent No 5,880,971, and Mader, US Patent No. 4,701,860.

In reference to claims 38 and 39, Guruswamy in view of Crafts and Dangelo teach the limitations of claims 33 and 37 as outlined above. They do not teach wherein

each sub-circuit performs one of a plurality of functions or that at least two sub-circuits having the different sizes and shapes perform the same logic function. Mader teaches wherein each sub-circuit performs one of a plurality of functions or that at least two sub-circuits having the different sizes and shapes perform the same logic function (column 8, lines 30-58). Accordingly it would have been obvious for one skilled in the art at the time of invention to incorporate the teachings of Mader with the teachings of Guruswamy in view of Crafts and Dangelo to make a method containing all the limitations of claims 33 and 37-39 because it would minimize the geometry size of the integrated circuit being designed.

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guruswamy et al., US Patent No. 5,984,510 in view of Crafts, US Patent No. 5,671,397, and Dangelo et al, US Patent No 5,880,971, and Chih et al., US Patent No. 4,584,653. Guruswamy in view of Crafts and Dangelo teach the limitations of claims 33 and 40 as outlined above. They do not teach wherein each sub-circuit is defined by at least one GDSII file. Chih teaches wherein each sub-circuit is defined by at least one GDSII file (column 8, lines 27-54). Accordingly it would have been obvious for one skilled in the art at the time of invention to incorporate the teachings of Chih with the teachings of Guruswamy in view of Crafts and Dangelo to make a method containing all the limitations of claims 33, and 40-41 because the Designer IV graphics system is being used.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W Bowers whose telephone number is (571)272-1888. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BWB

VUTHE SIEK
PRIMARY EXAMINER